FIG. 1

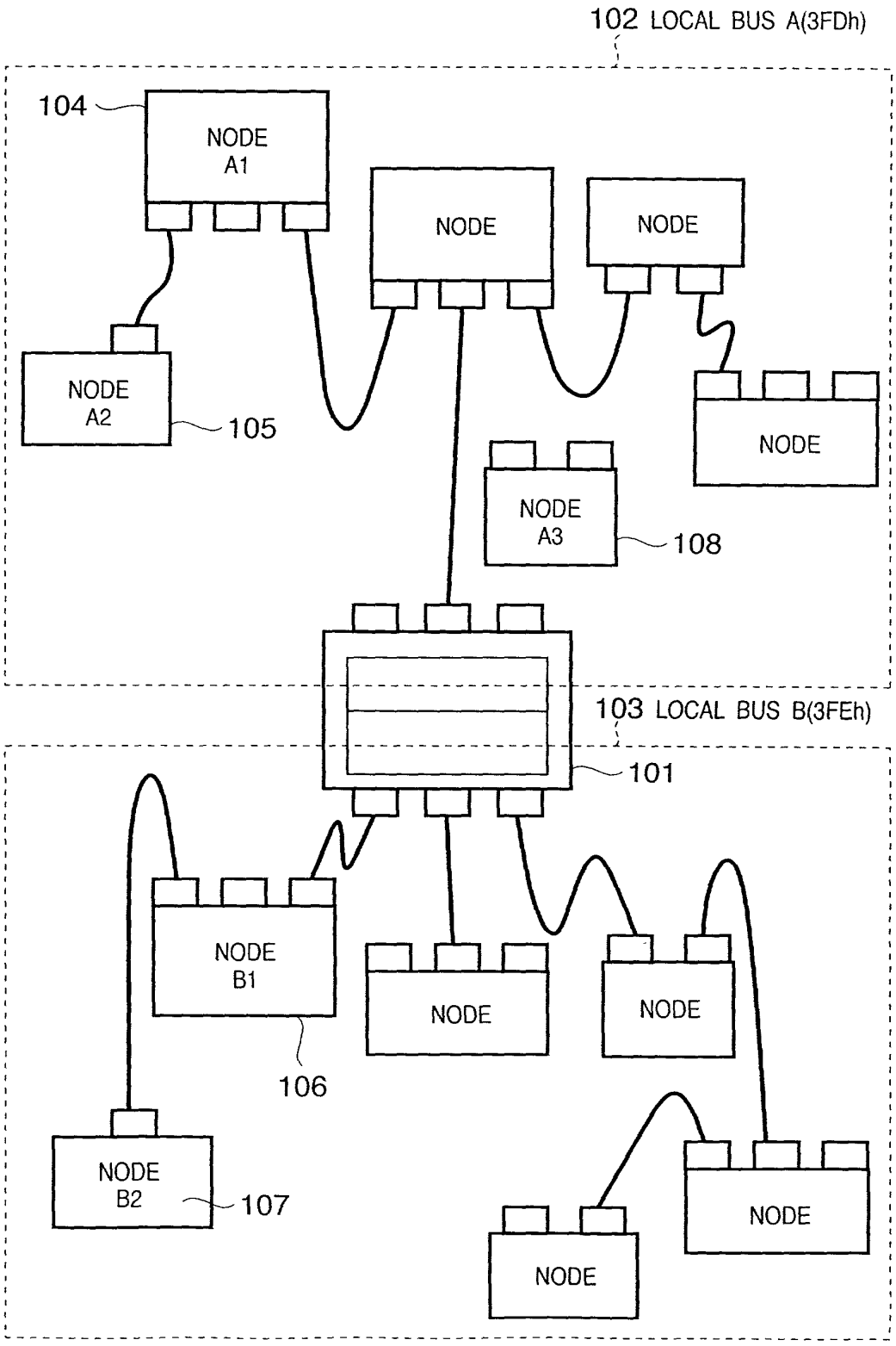

102 LOCAL BUS A(3FDh)
104
NODE A1
NODE
NODE
NODE A2
105
NODE
NODE A3
108
103 LOCAL BUS B(3FEh)
101
NODE B1
NODE
NODE
106
NODE B2
107
NODE
NODE

FIG. 2

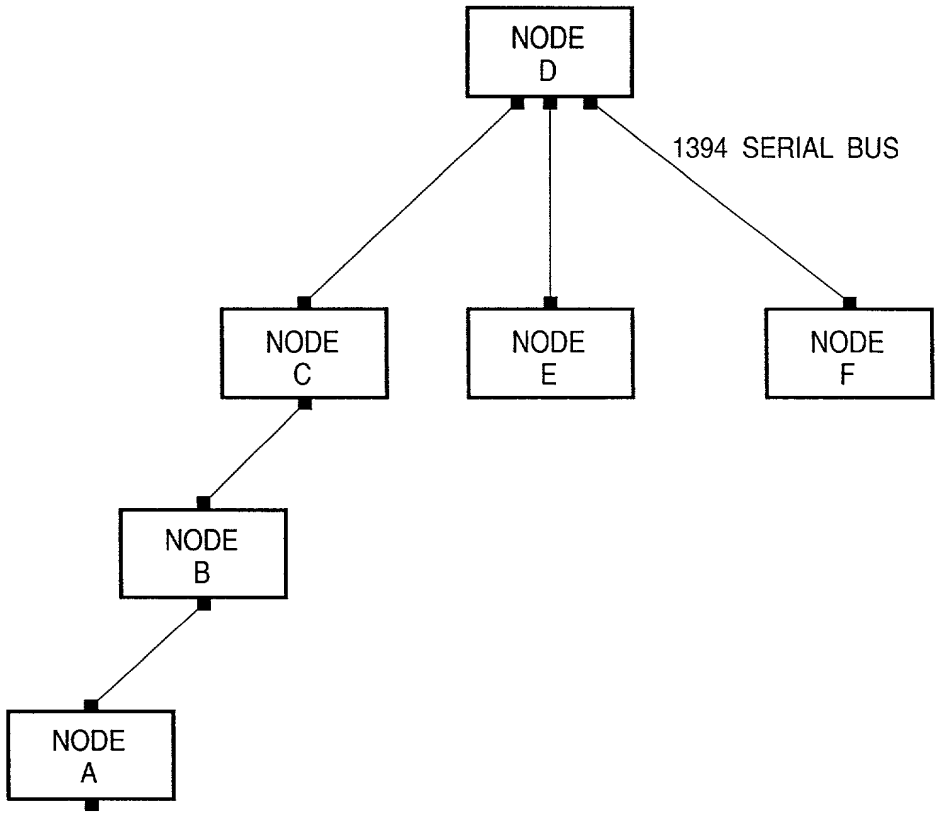


FIG. 3

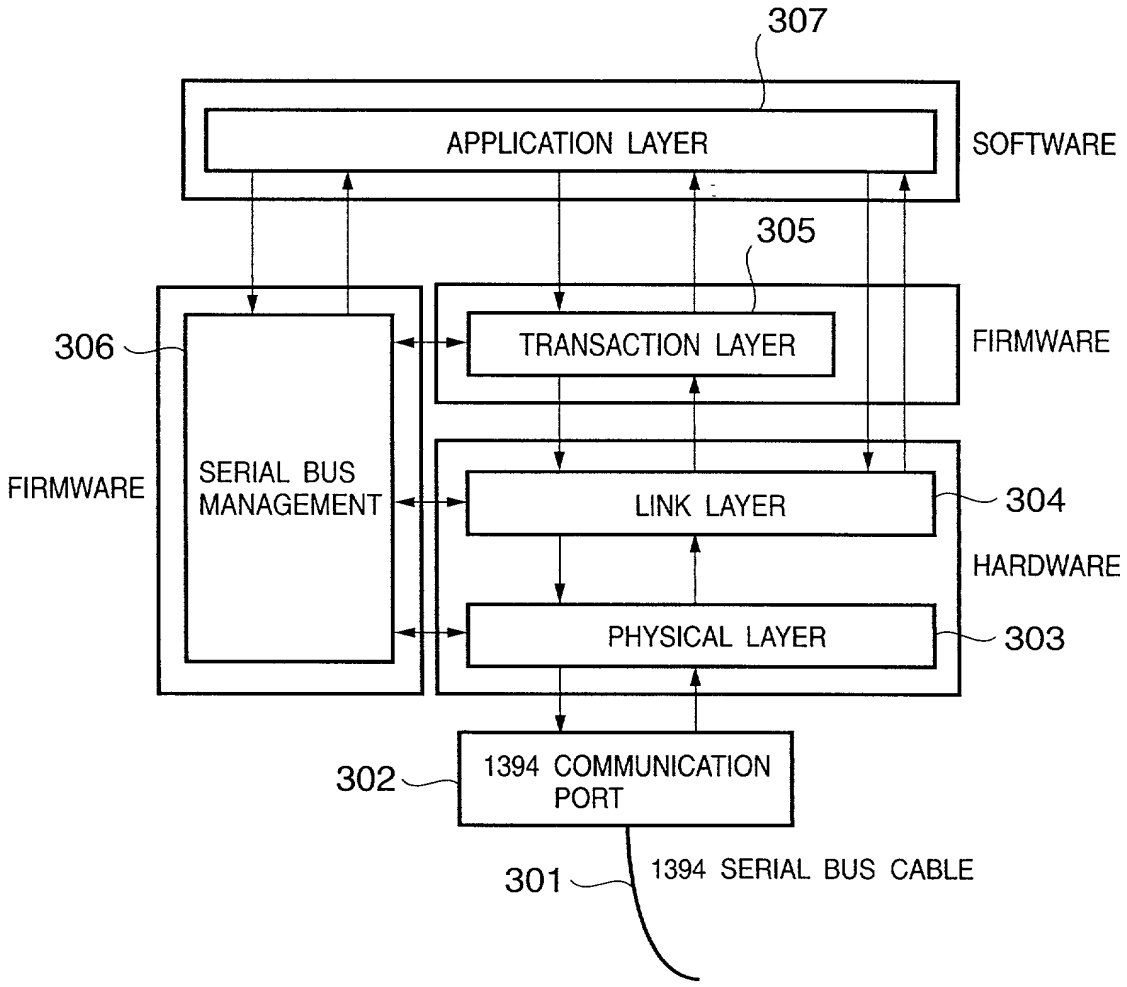

307
APPLICATION LAYER
SOFTWARE
305
306
TRANSACTION LAYER
FIRMWARE
FIRMWARE
SERIAL BUS MANAGEMENT
LINK LAYER
304
HARDWARE
PHYSICAL LAYER
303
302
1394 COMMUNICATION PORT
301
1394 SERIAL BUS CABLE

FIG. 4

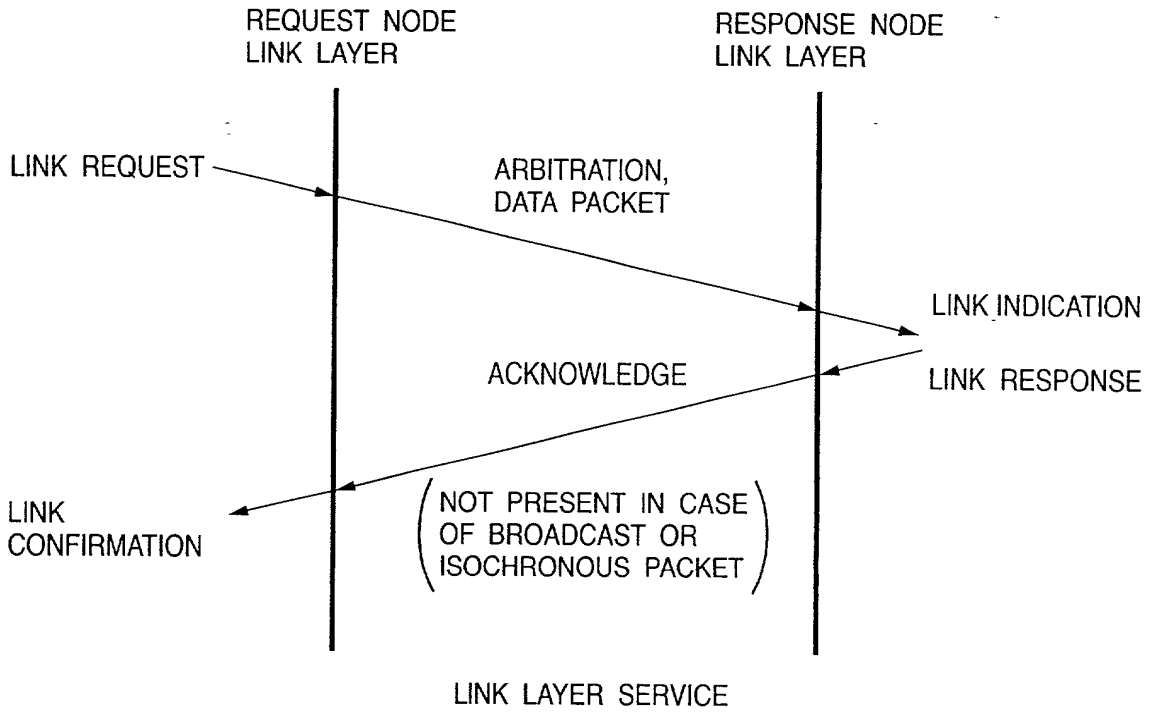

REQUEST NODE
LINK LAYER
RESPONSE NODE
LINK LAYER
LINK REQUEST
ARBITRATION,
DATA PACKET
LINK INDICATION
ACKNOWLEDGE
LINK RESPONSE
LINK
CONFIRMATION
NOT PRESENT IN CASE
OF BROADCAST OR
ISOCHRONOUS PACKET
LINK LAYER SERVICE

FIG. 5

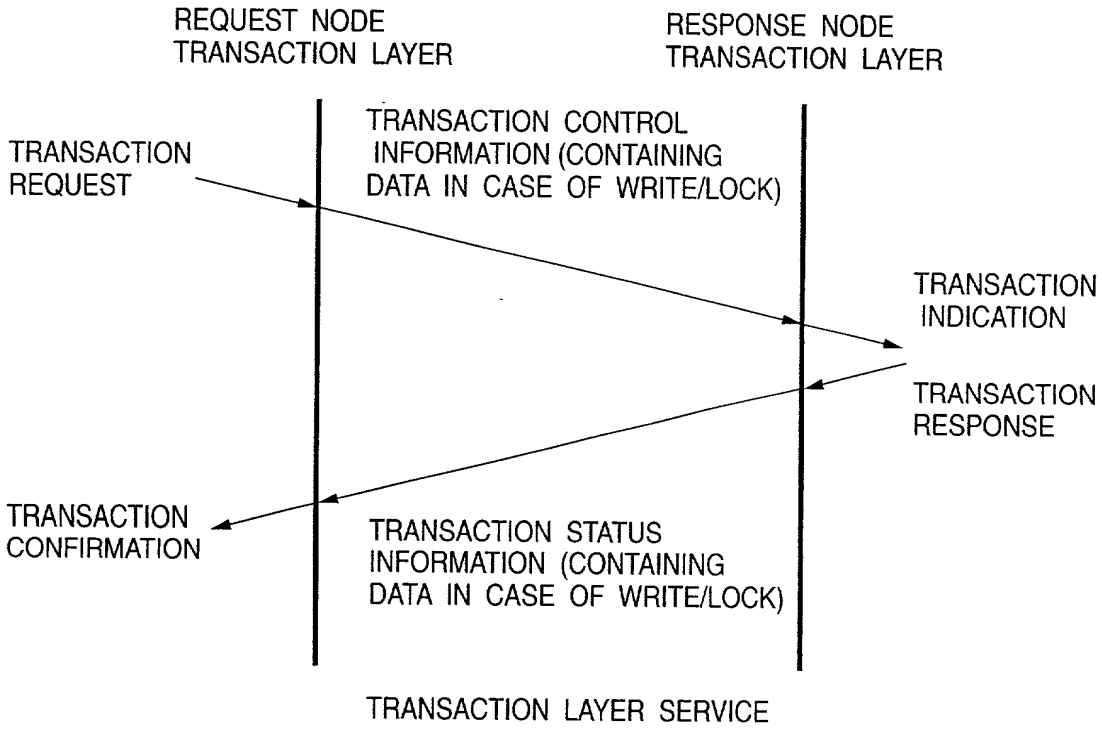

REQUEST NODE
TRANSACTION LAYER
RESPONSE NODE
TRANSACTION LAYER
TRANSACTION
REQUEST
TRANSACTION CONTROL
INFORMATION (CONTAINING
DATA IN CASE OF WRITE/LOCK)
TRANSACTION
INDICATION
TRANSACTION
RESPONSE
TRANSACTION
CONFIRMATION
TRANSACTION STATUS
INFORMATION (CONTAINING
DATA IN CASE OF WRITE/LOCK)
TRANSACTION LAYER SERVICE

FIG. 6

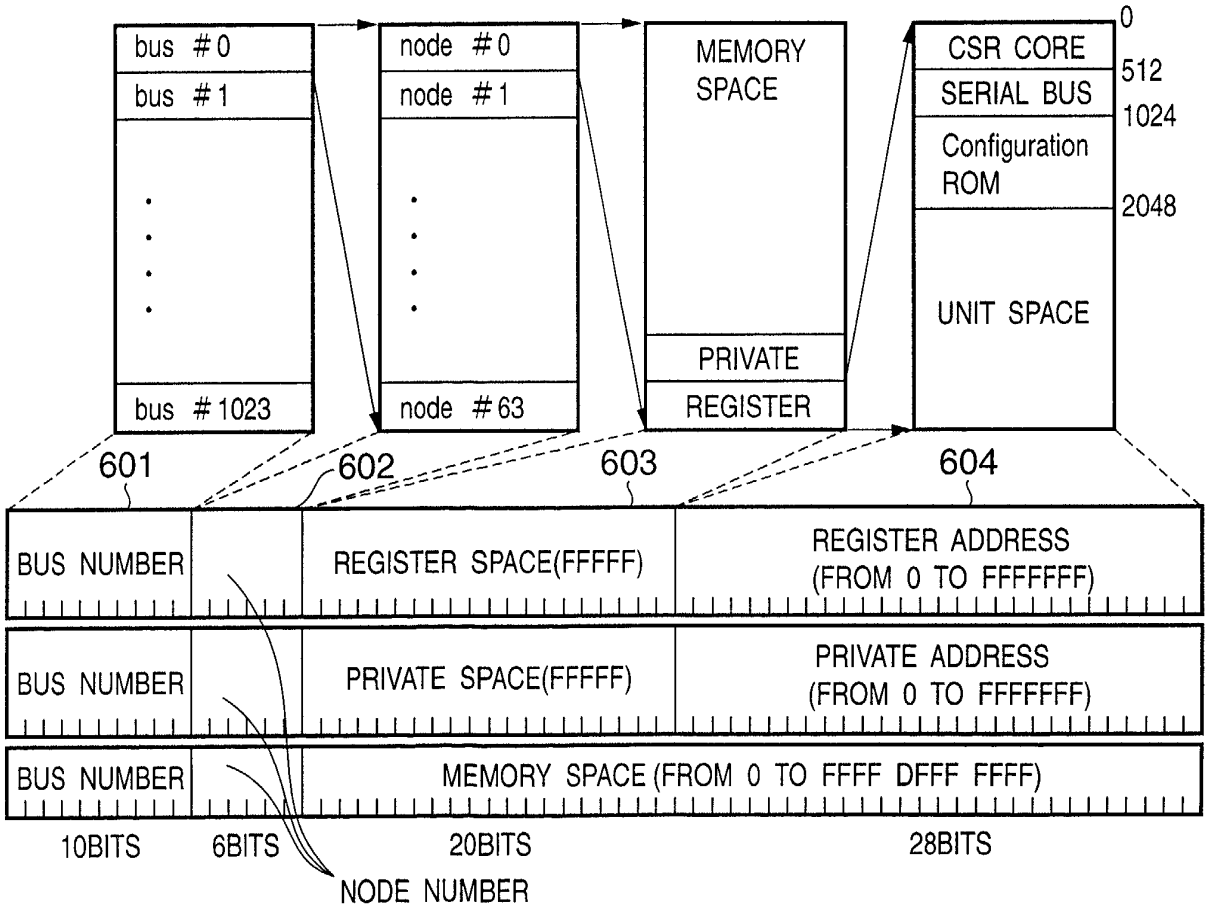

bus #0
bus #1
bus #1023
node #0
node #1
node #63
MEMORY SPACE
PRIVATE
REGISTER
0
CSR CORE
512
SERIAL BUS
1024
Configuration ROM
2048
UNIT SPACE
601
602
603
604
BUS NUMBER
REGISTER SPACE(FFFFF)
REGISTER ADDRESS (FROM 0 TO FFFFFFF)
BUS NUMBER
PRIVATE SPACE(FFFFF)
PRIVATE ADDRESS (FROM 0 TO FFFFFFF)
BUS NUMBER
MEMORY SPACE (FROM 0 TO FFFF DFFF FFFF)
10BITS
6BITS
20BITS
28BITS
NODE NUMBER

FIG. 7

CSR CORE REGISTER

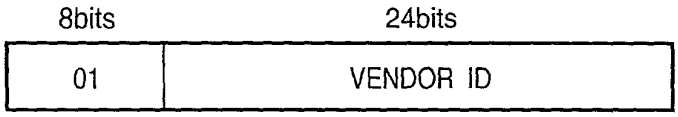
OFFSET (HEXADECIMAL)	REGISTER NAME	FUNCTION
000	STATE_CLEAR	INFORMATION OF STATUS AND CONTROL
004	STATE_SET	INFORMATION INDICATING WRITE ENABLE/DISABLE OF STATE_CLEAR
008	NODE_IDS	BUS ID + NODE ID
00C	RESET_START	RESET BUS BY WRITE IN THIS AREA
010~014	INDIRECT_ADDRESS, INDIRECT_DATA	REGISTER FOR ACCESSING ROM LARGER THAN 1K
018~01C	SPLIT_TIMEOUT	VALUE OF TIMER FOR DETECTING TIME-OUT OF SPLIT TRANSACTION
020~02C	ARGUMENT,TEST_START, TEST_STATUS	DIAGNOSIS REGISTER
030~04C	UNITS_BASE,UNITS_BOUND, MEMORY_BASE, MEMORY_BOUND	NOT USED IN IEEE1394
050~054	INTERRUPT_TARGET, INTERRUPT_MASK	INTERRUPT INDICATION REGISTER
058~07C	CLOCK_VALUE, CLOCK_TICK_PERIOD, CLOCK_STOROBE_ARRIVED, CLOCK_INFO	NOT USED IN IEEE1394
080~0FC	MESSAGE_REQUEST, MESSAGE_RESPONSE	MESSAGE INDICATION REGISTER
100~17C		RESERVED
180~1FC	ERROR_LOG_BUFFER	RESERVED FOR IEEE1394

FIG. 8

SERIAL BUS REGISTER

OFFSET (HEXADECIMAL)	REGISTER NAME	FUNCTION
200	CYCLE_TIME	COUNTER FOR ISOCHRONOUS TRANSFER
204	BUS_TIME	REGISTER FOR SYNCHRONIZING TIME
208	POWER_FAIL_IMMINENT	REGISTER ASSOCIATED WITH POWER SUPPLY
20C	POWER_SOURCE	
210	BUSY_TIMEOUT	CONTROL RETRY OF TRANSACTION LAYER
214~218		RESERVED
21C	BUS_MANAGER_ID	NODE ID OF BUS MANAGER
220	BANDWIDTH_AVAILABLE	MANAGE BANDWIDTH OF ISOCHRONOUS TRANSFER
224~228	CHANNELS_AVAILABLE	MANAGE CHANNEL NUMBER OF ISOCHRONOUS TRANSFER
22C	MAINT_CONTROL	DIAGNOSIS REGISTER
230	MAINT_UTILITY	
234~3FC		RESERVED

FIG. 9



CONFIGURATION ROM OF MINIMAL FORMAT

FIG. 10

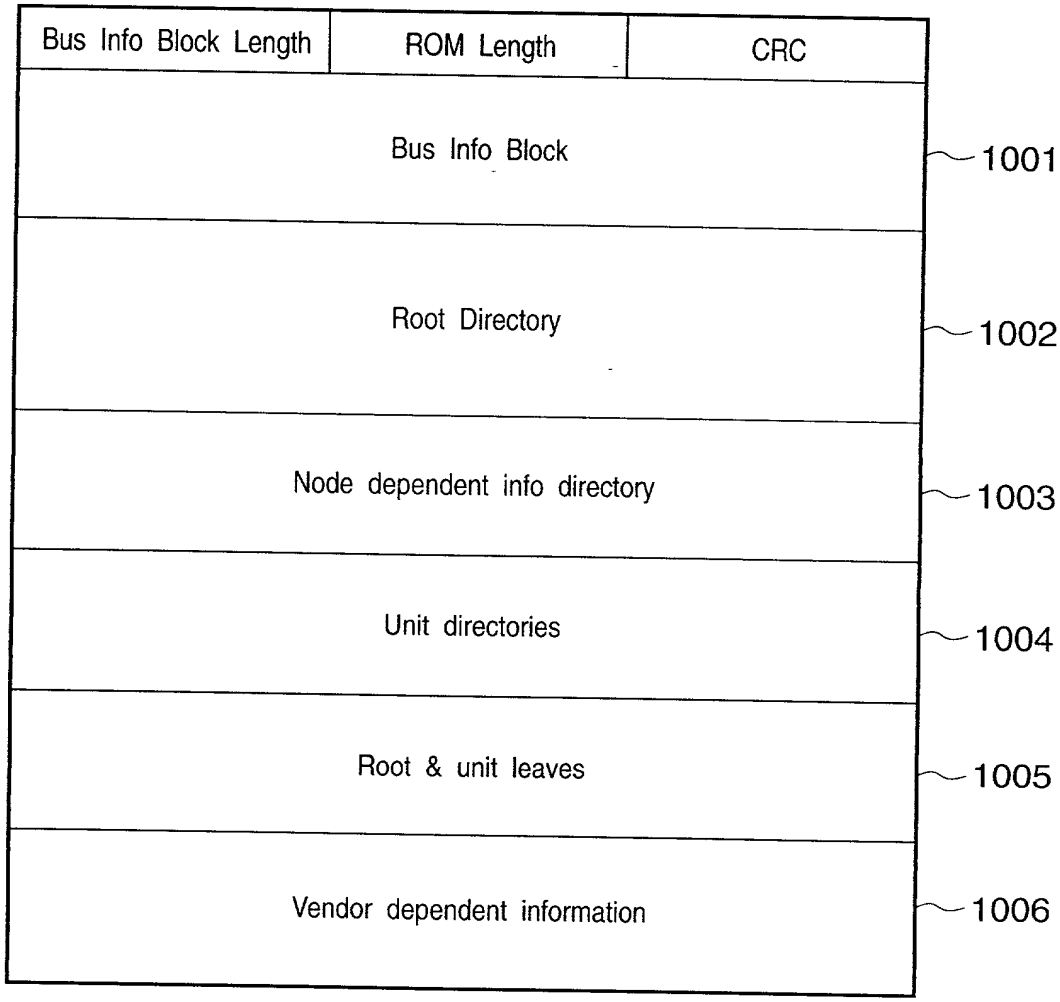
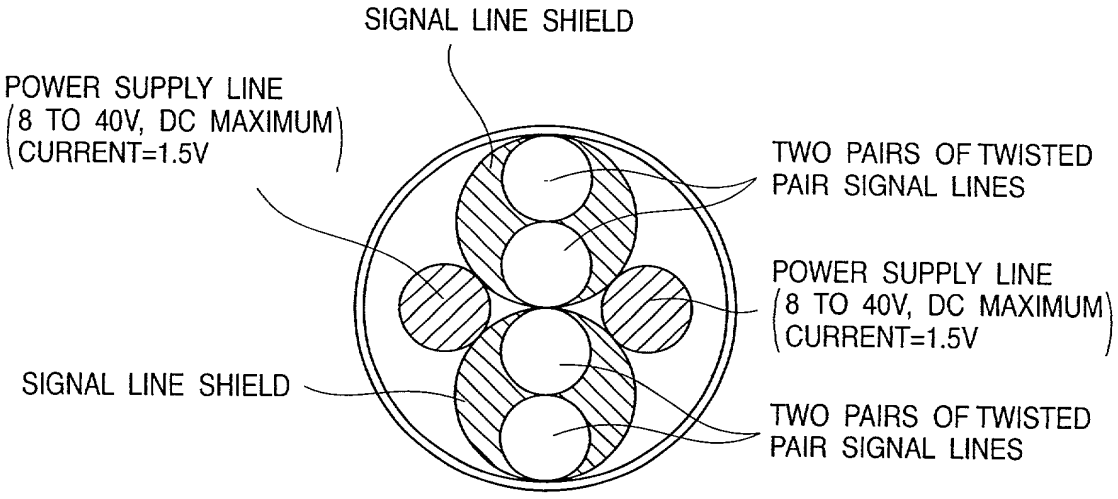

Bus Info Block Length
ROM Length
CRC
Bus Info Block
1001
Root Directory
1002
Node dependent info directory
1003
Unit directories
1004
Root & unit leaves
1005
Vendor dependent information
1006

FIG. 11

SERIAL BUS DEVICE REGISTER

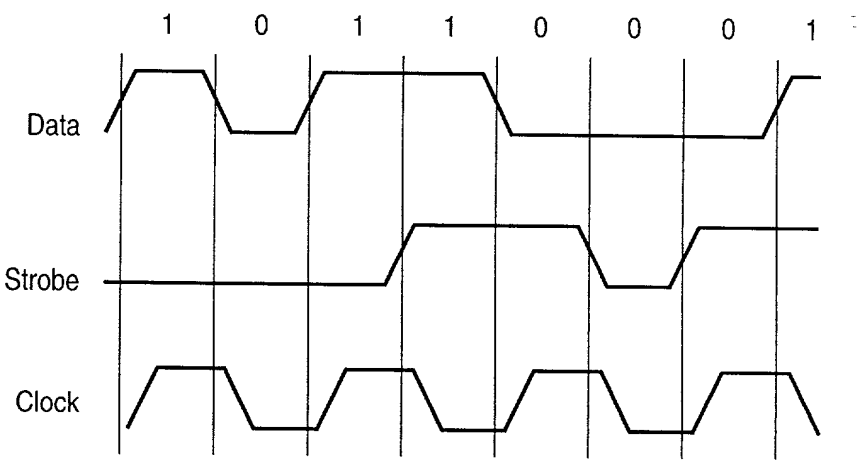
OFFSET (HEXADECIMAL)	REGISTER NAME	FUNCTION
800~FFC		RESERVED
1000~13FC	TOPOLOGY_MAP	CONFIGURATION INFORMATION OF SERIAL BUS
1400~1FFC		RESERVED
2000~2FFC	SPEED_MAP	INFORMATION OF TRANSFER RATE OF SERIAL BUS
3000~FFFC		RESERVED

FIG. 12



CABLE SECTIONAL VIEW

FIG. 13



EX-OR SIGNAL OF DATA AND STROBE

FIG. 14

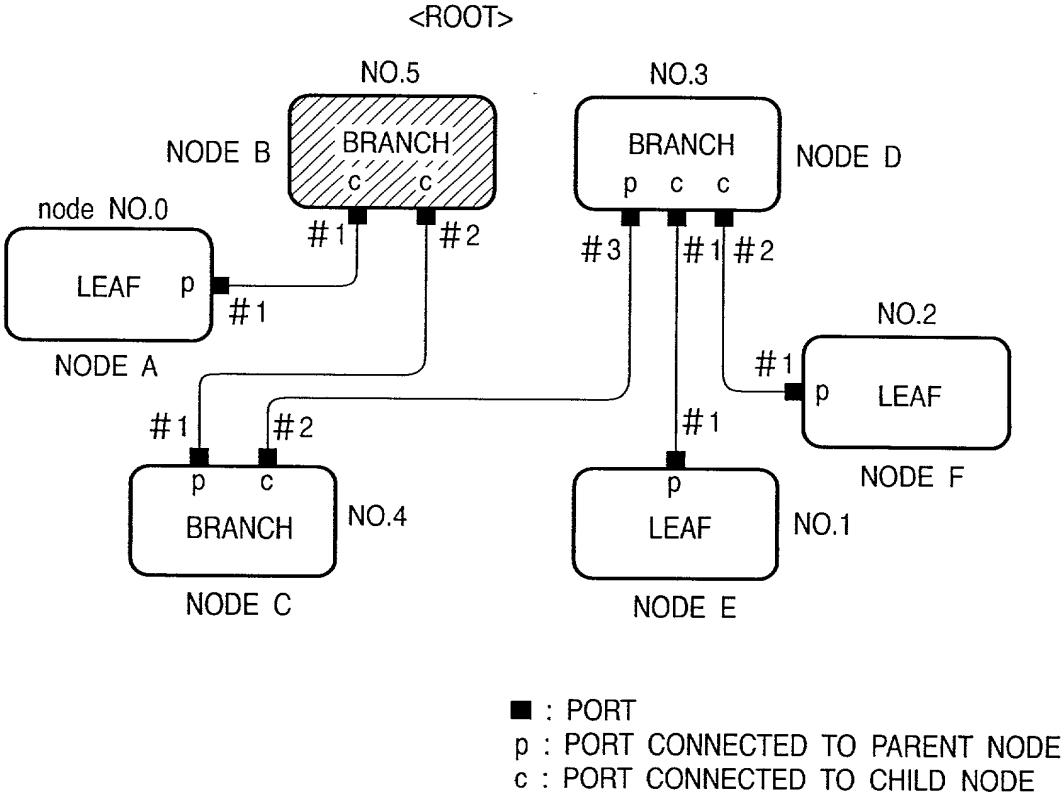

<ROOT>
NO.5
NODE B
BRANCH
c c
#1 #2
node NO.0
LEAF p
#1
NODE A
NO.3
BRANCH
p c c
NODE D
#3 #1 #2
NO.2
#1
p LEAF
NODE F
#1 #2
p c
BRANCH
NO.4
NODE C
#1
p
LEAF
NO.1
NODE E
■ : PORT
p : PORT CONNECTED TO PARENT NODE
c : PORT CONNECTED TO CHILD NODE

FIG. 15

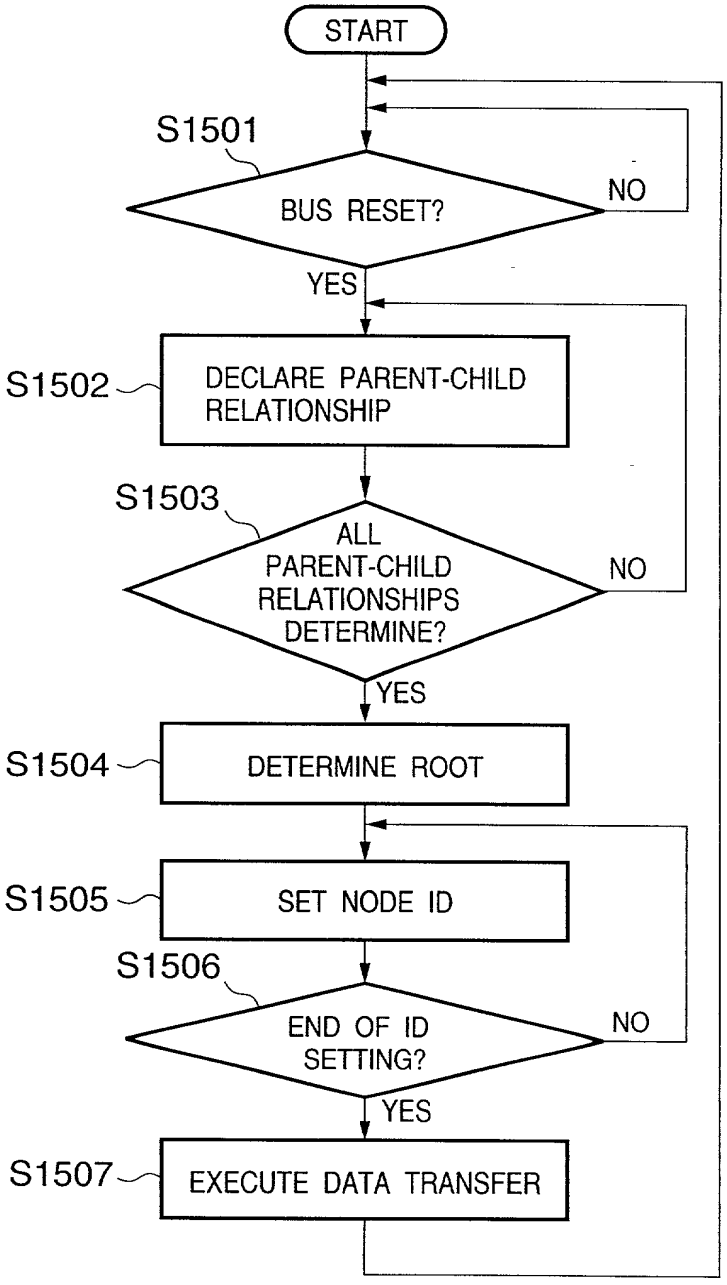
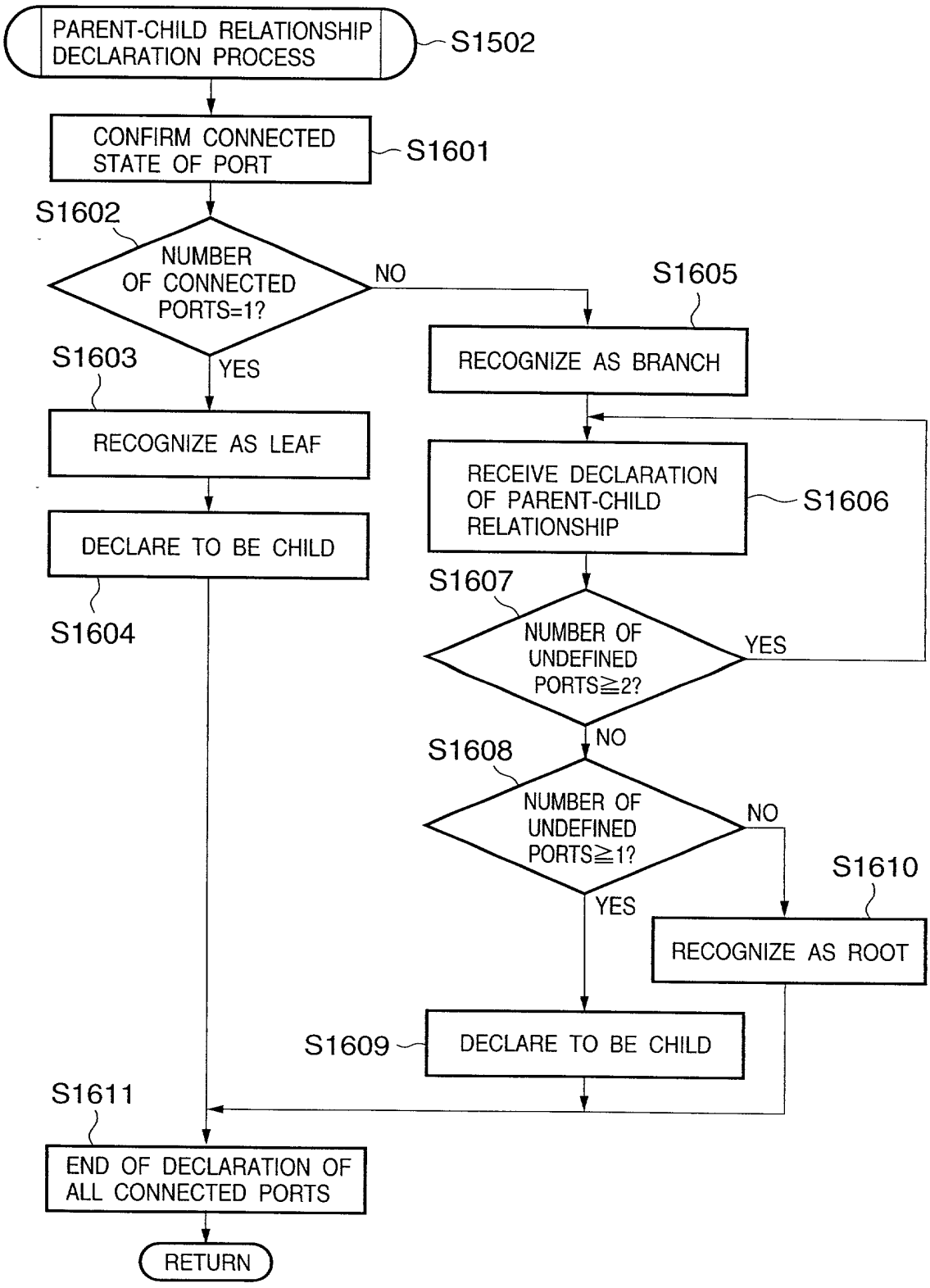

START
S1501
BUS RESET?
NO
YES
S1502
DECLARE PARENT-CHILD RELATIONSHIP
S1503
ALL PARENT-CHILD RELATIONSHIPS DETERMINE?
NO
YES
S1504
DETERMINE ROOT
S1505
SET NODE ID
S1506
END OF ID SETTING?
NO
YES
S1507
EXECUTE DATA TRANSFER

FIG. 16


PARENT-CHILD RELATIONSHIP DECLARATION PROCESS
S1502
CONFIRM CONNECTED STATE OF PORT
S1601
S1602
NUMBER OF CONNECTED PORTS=1?
NO
S1605
YES
S1603
RECOGNIZE AS BRANCH
RECOGNIZE AS LEAF
RECEIVE DECLARATION OF PARENT-CHILD RELATIONSHIP
S1606
DECLARE TO BE CHILD
S1607
S1604
NUMBER OF UNDEFINED PORTS≧2?
YES
NO
S1608
NUMBER OF UNDEFINED PORTS≧1?
NO
S1610
YES
RECOGNIZE AS ROOT
S1609
DECLARE TO BE CHILD
S1611
END OF DECLARATION OF ALL CONNECTED PORTS
RETURN

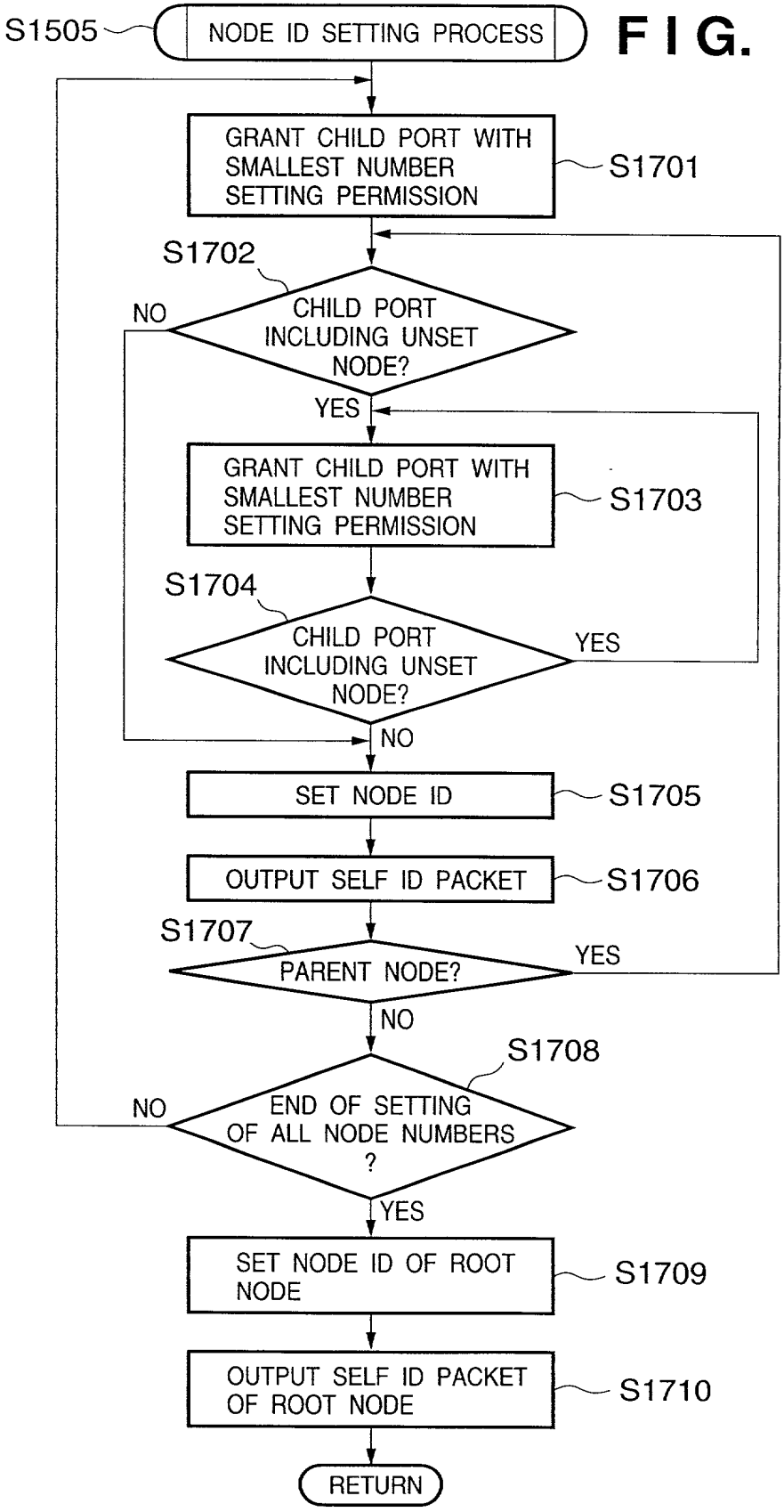

S1505
NODE ID SETTING PROCESS
GRANT CHILD PORT WITH SMALLEST NUMBER SETTING PERMISSION
S1701
S1702
CHILD PORT INCLUDING UNSET NODE?
NO
YES
GRANT CHILD PORT WITH SMALLEST NUMBER SETTING PERMISSION
S1703
S1704
CHILD PORT INCLUDING UNSET NODE?
YES
NO
SET NODE ID
S1705
OUTPUT SELF ID PACKET
S1706
S1707
PARENT NODE?
YES
NO
S1708
END OF SETTING OF ALL NODE NUMBERS ?
NO
YES
SET NODE ID OF ROOT NODE
S1709
OUTPUT SELF ID PACKET OF ROOT NODE
S1710
RETURN

FIG. 17

FIG. 18

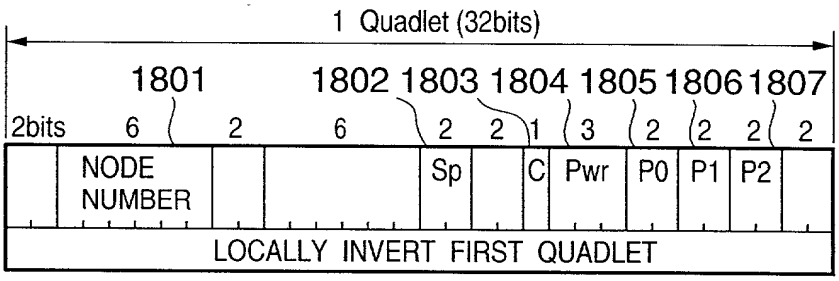
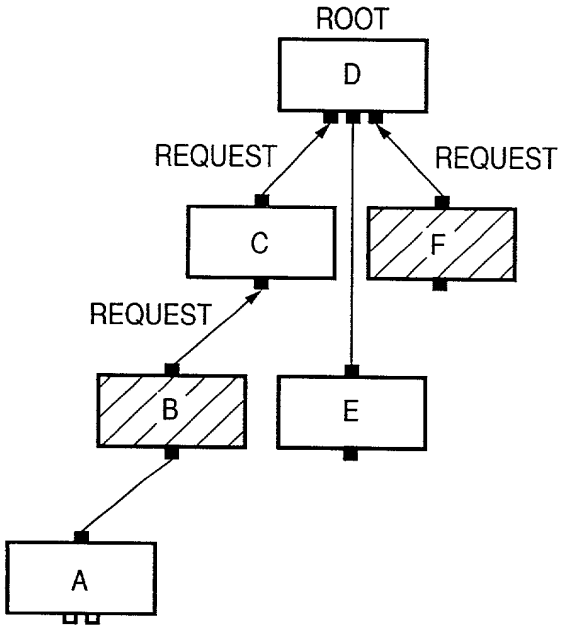
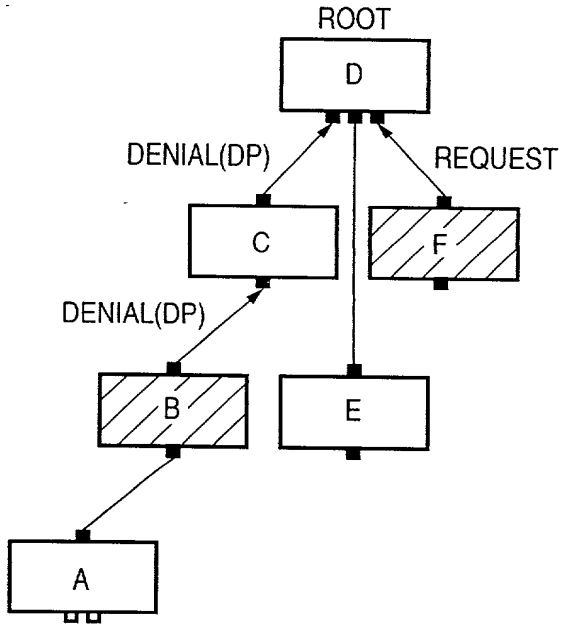

1 Quadlet (32bits)
1801
1802
1803
1804
1805
1806
1807
2bits
6
2
6
2
2
1
3
2
2
2
2
NODE NUMBER
Sp
C
Pwr
P0
P1
P2
LOCALLY INVERT FIRST QUADLET

FIG. 19A



REQUEST RIGHT TO USE BUS

FIG. 19B



PERMIT RIGHT TO USE BUS

FIG. 20

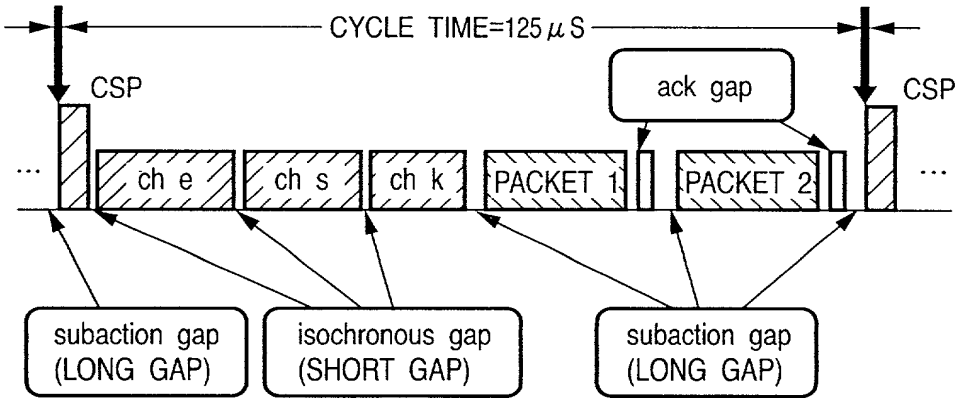
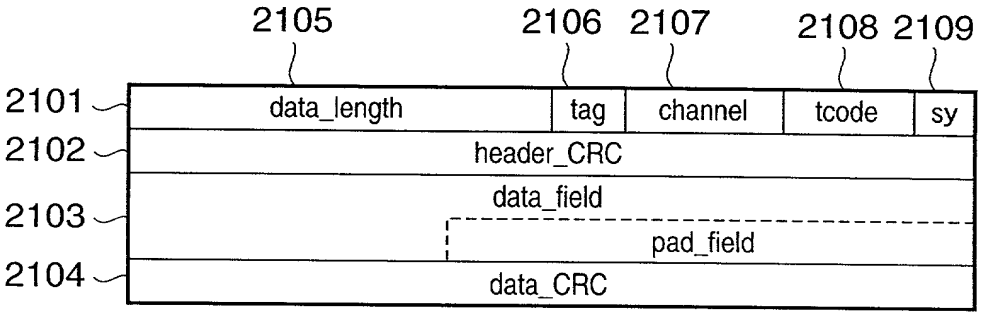

CYCLE TIME=125 μ S
CSP
ack gap
CSP
ch e
ch s
ch k
PACKET 1
PACKET 2
subaction gap
(LONG GAP)
isochronous gap
(SHORT GAP)
subaction gap
(LONG GAP)

FIG. 21



PACKET OF ISOCHRONOUS DATA

FIG. 22

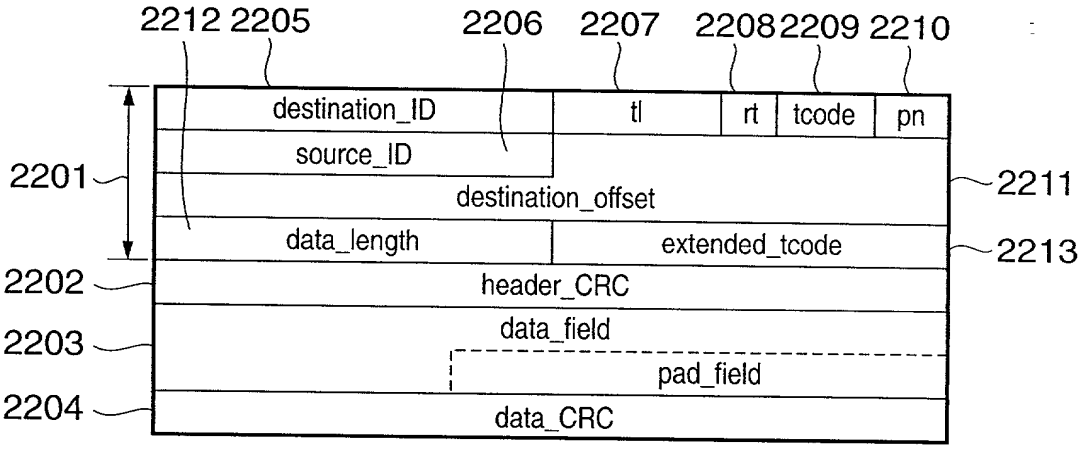

2212 2205
2206
2207
2208 2209 2210
destination_ID
tl
rt
tcode
pn
source_ID
destination_offset
data_length
extended_tcode
header_CRC
data_field
pad_field
data_CRC
2201
2202
2203
2204
2211
2213

FIG. 23

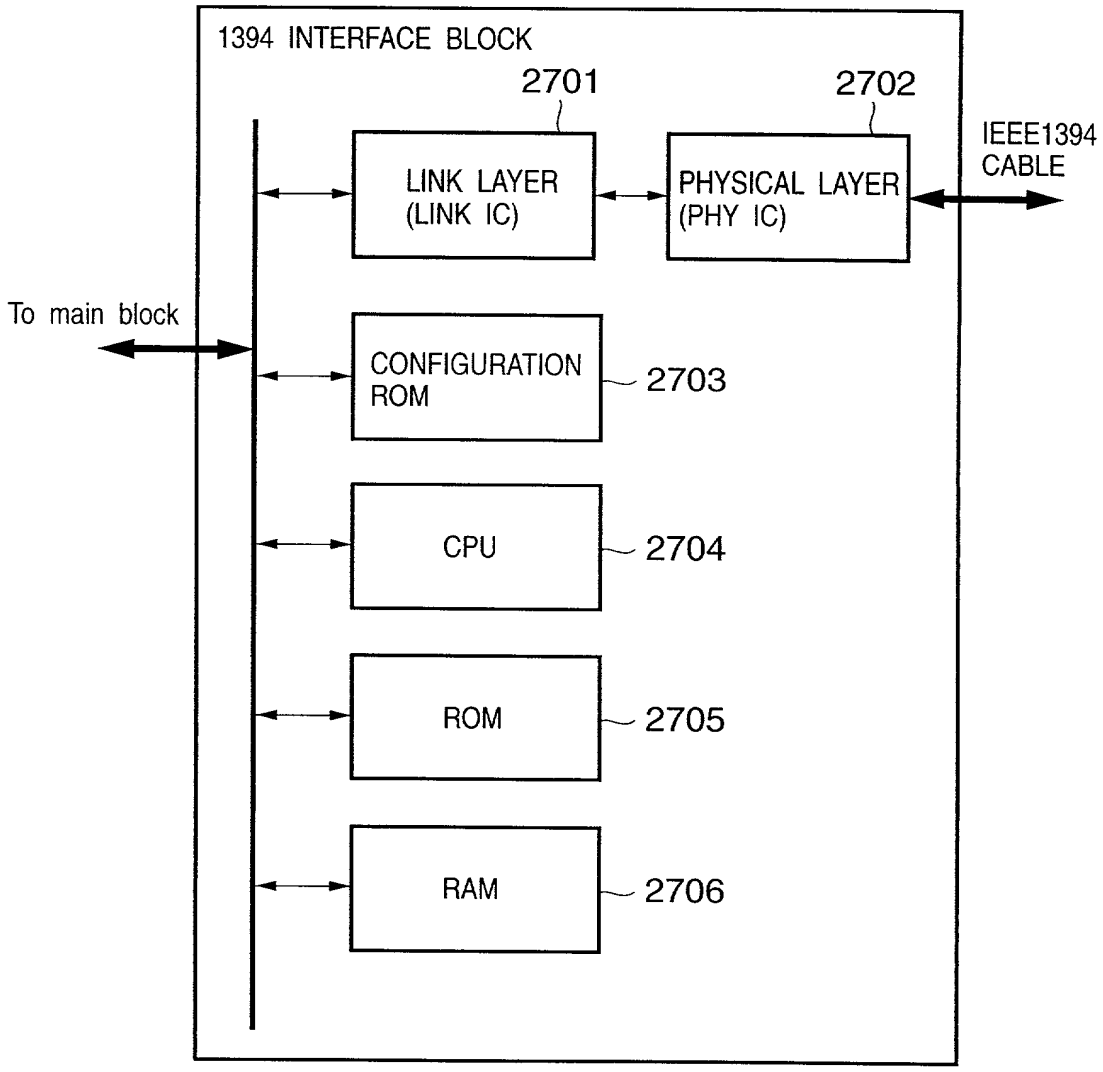

1394 INTERFACE BLOCK
2701
2702
LINK LAYER
(LINK IC)
PHYSICAL LAYER
(PHY IC)
IEEE1394
CABLE
To main block
CONFIGURATION
ROM
2703
CPU
2704
ROM
2705
RAM
2706

FIG. 24

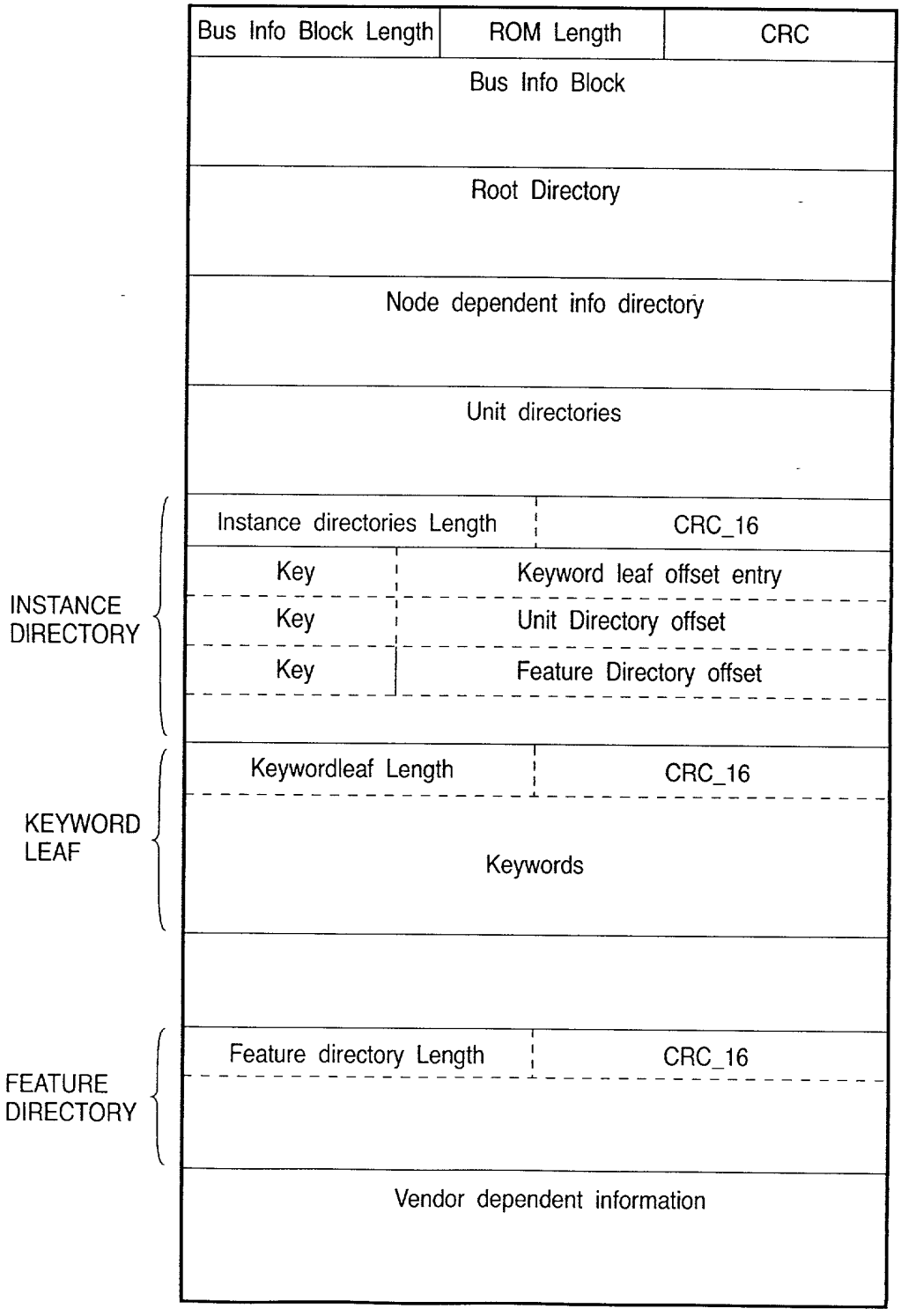

Bus Info Block Length
ROM Length
CRC
Bus Info Block
Root Directory
Node dependent info directory
Unit directories
INSTANCE DIRECTORY
Instance directories Length
CRC_16
Key
Keyword leaf offset entry
Key
Unit Directory offset
Key
Feature Directory offset
KEYWORD LEAF
Keywordleaf Length
CRC_16
Keywords
FEATURE DIRECTORY
Feature directory Length
CRC_16
Vendor dependent information

FIG. 25

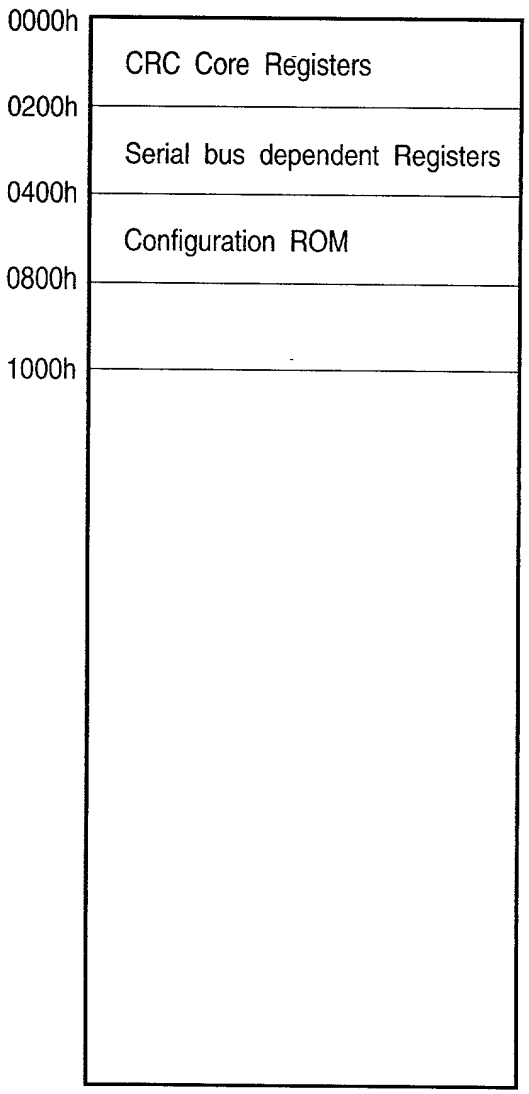


FIG. 26

SERIAL BUS REGISTER

OFFSET (HEXADECIMAL)	REGISTER NAME	FUNCTION
200	CYCLE_TIME	COUNTER FOR ISOCHRONOUS TRANSFER
204	BUS_TIME	REGISTER FOR SYNCHRONIZING TIME
208	POWER_FAIL_IMMINENT	REGISTER ASSOCIATED WITH POWER SUPPLY
20C	POWER_SOURCE	
210	BUSY_TIMEOUT	CONTROL RETRY OF TRANSACTION LAYER
214～218		RESERVED
21C	BUS_MANAGER_ID	NODE TRANSFER OF BUS MANAGER
220	BANDWIDTH_AVAILABLE	MANAGE BANDWIDTH OF ISOCHRONOUS TRANSFER
224～228	CHANNELS_AVAILABLE	MANAGE CHANNEL NUMBER OF ISOCHRONOUS TRANSFER
22C	MAIN_CONTROL	DIAGNOSIS REGISTER
230	MAIN_UTILITY	
234～23C		RESERVED
240	REMOTE_BUS_RESET	INDICATE BUS RESET IN REMOTE BUS
244	EVENT_CONTROL	MANAGE EVENTS

FIG. 27

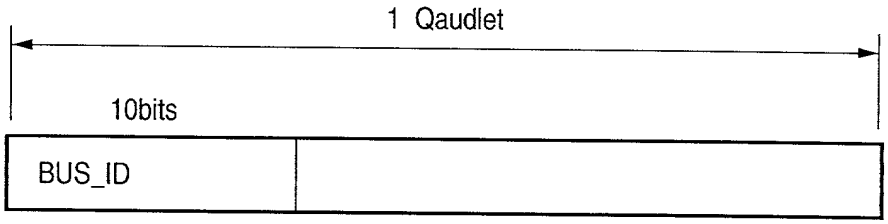


FIG. 28

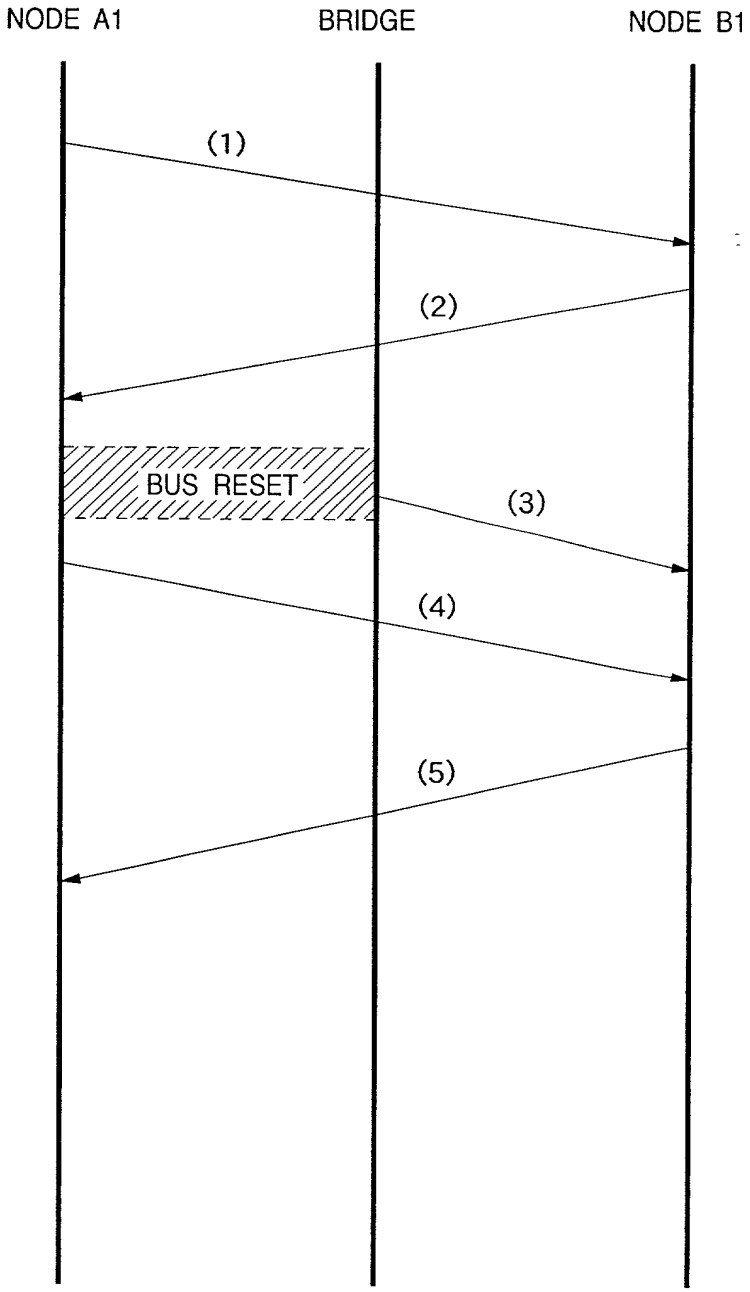


FIG. 29

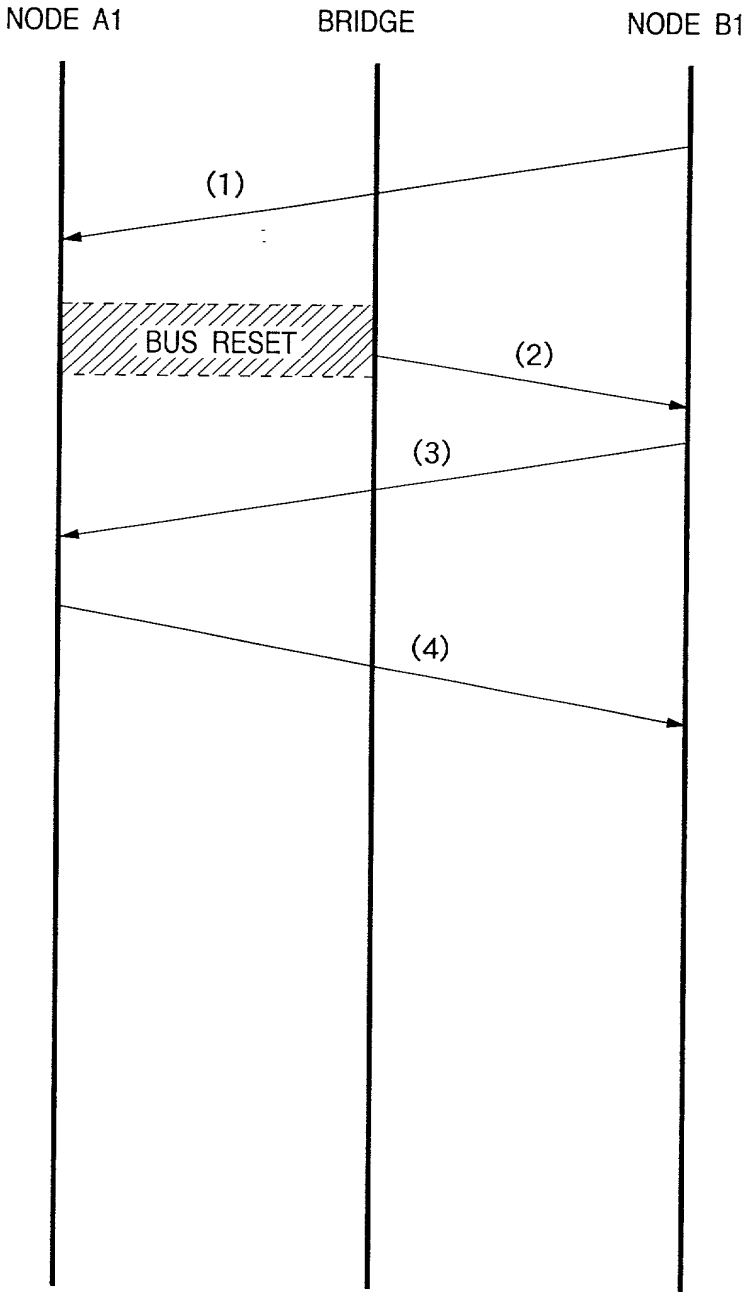
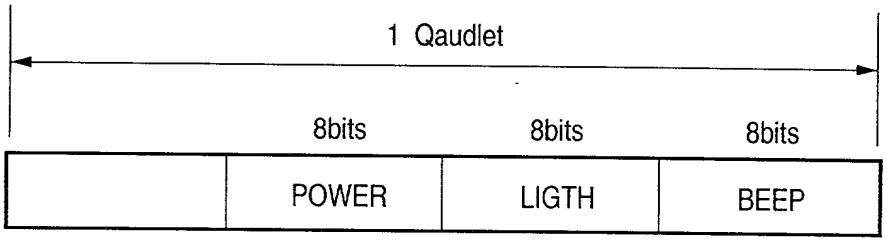


FIG. 30

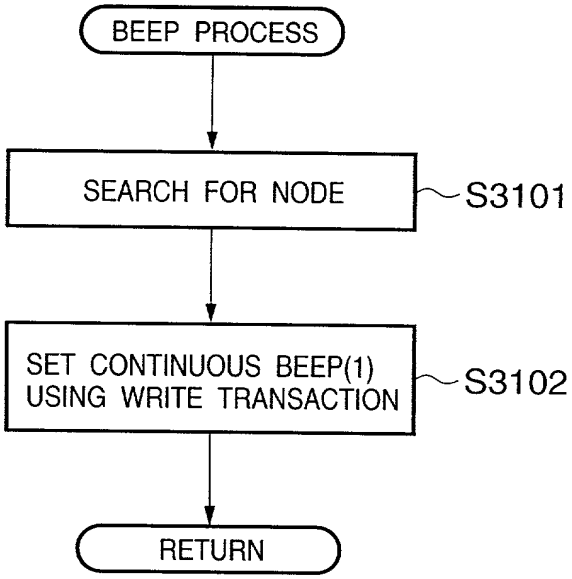


BEEP = 0 NOT BEEP
1 CONTINUOUSLY BEEP
2 INTERMITTENTLY BEEP

LIGHT = 0 NOT EMIT LIGHT
1 EMIT LIGHT
2 FLICKER

POWER = 0 NOT CONTROL
1 TURN ON POWER SUPPLY
2 TURN OFF POWER SUPPLY

FIG. 31


BEEP PROCESS
SEARCH FOR NODE
S3101
SET CONTINUOUS BEEP(1)
USING WRITE TRANSACTION
S3102
RETURN